Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (original) A direct current to direct current converter, comprising:

a first switch, the first switch to output a first voltage on a first output terminal in response to a turn-on voltage at a first control terminal, wherein the first control terminal selectively communicates with one of N > 2 different voltages; and

a second switch, the second switch to output a second voltage on a second output terminal in communication with the first output terminal in response to a turn-on voltage at a second control terminal, wherein the second control terminal selectively communicates with one of M > 1 different voltages.

2. (original) The converter of claim 1, wherein M is greater than two.

3. (original) The converter of claim 1, wherein the first output terminal and the second output terminal are in communication with a load.

4. (original) The converter of claim 3, wherein the first output terminal and the second output terminal are in communication with the load via an inductor and a capacitor.

5. (original) The converter of claim 1, wherein the first switch comprises a first transistor, the first output terminal comprises a drain of the first transistor, and the first control terminal comprises a gate of the first transistor.

6. (original) The converter of claim 1, further including N voltage sources each supplying one of the N different voltages.

7. (original) The converter of claim 1, wherein the first switch comprises a transistor having a source and a drain, and further comprising a voltage detector to detect a potential difference between the source and the drain.

8. (original) The converter of claim 7, further including a switch assembly controller responsive to the voltage detector and further in communication with the first control terminal, and wherein the first control terminal selectively communicates with the one of the $N > 2$ different voltages in accordance with the switch assembly controller.

9. (original) The converter of claim 1, further including a first multi-level controller in communication with the first control terminal, the first multi-level controller including N drivers, each of the n=1 to n=N drivers to selectively apply a different voltage V_n of the N different voltages to the first control terminal.

10. (original) The converter of claim 9, further including a second multi-level controller in communication with the second control terminal, the second multi-level controller including M drivers, each of the m=1 to m=M drivers to selectively apply a different voltage V_m of the M different voltages to the second control terminal.

11. (original) The converter of claim 10, wherein the first multi-level controller and the second multi-level controller are to turn on the first switch and the second switch alternately.

12. (original) The converter of claim 9, wherein the first multi-level controller comprises a switching mechanism to selectively communicate the N > 2 different applied voltages with the first control terminal.

13. (original) The converter of claim 9, wherein at least one of the N drivers comprises an associated capacitance.

14. (original) The converter of claim 13, wherein at least a portion of the first multi-level controller is included in an integrated circuit, and wherein an associated capacitance of at least one of the N drivers includes a capacitance of a capacitor not included in the integrated circuit.

15. (original) The converter of claim 14, wherein the first switch comprises a transistor with a gate and a source having an associated capacitance C_{gs}, and wherein the capacitance of the capacitor not included in the integrated circuit is larger than C_{gs}.

16. (original) The converter of claim 9, wherein the first switch comprises a PMOS transistor, wherein the first control terminal is a gate of the PMOS transistor, and wherein the N drivers comprise three drivers to selectively apply a voltage V_1 at which the PMOS transistor is off, a voltage V_3 at which the PMOS transistor is on, and an intermediate voltage V_2 between V_1 and V_3.

17. (original) The converter of claim 16, wherein V_1 is about equal to negative five volts or less, and wherein V_3 is ground.

18. (original) The converter of claim 16, wherein the N drivers further comprise a fourth driver to selectively apply another intermediate voltage V_4, and wherein V_4 is between V_1 and V_3.

19. (original) The converter of claim 9, wherein the first switch comprises an NMOS transistor, wherein the first control terminal is a gate of the NMOS transistor, and wherein the N drivers comprise three drivers to selectively apply a voltage V_1 at which the NMOS transistor is on, a voltage V_3 at which the NMOS transistor is off, and an intermediate voltage V_2 between V_1 and V_3.

20. (original) The converter of claim 19, wherein V_1 is equal to about five volts or greater, and wherein V_3 ground.

21. (original) The converter of claim 19, wherein the N drivers further comprise a fourth driver to selectively apply another intermediate voltage V_4, and wherein V_4 is between V_1 and V_3.

22. (original) The converter of claim 9, wherein the N drivers are to selectively apply the different voltage V_n for a time sufficient for the voltage at the first control terminal to substantially equilibrate with V_n.

23. (original) A direct current to direct current converter, comprising:

an integrated circuit, the integrated circuit including:

a first switch, the first switch to output a first voltage on a first output terminal in response to a turn-on voltage at a first control terminal;

a second switch, the second switch to output a second voltage on a second output terminal in communication with the first output terminal in response to a turn-on voltage at a second control terminal; and

a first multi-level controller in communication with the first control terminal, the first multi-level controller including N drivers, each of the n=1 to n=N drivers to selectively apply a different voltage V_n to the first control terminal, where N is greater than two, and wherein at least one of the N drivers comprises an associated capacitance; and

a capacitor separate from the integrated circuit, a capacitance of the capacitor included in the associated capacitance of one of the N drivers.

24. (original) The converter of claim 23, wherein the associated capacitance of the one of the N drivers further includes an on-chip capacitance of one or more elements of the integrated circuit.

25. (original) The converter of claim 23, wherein the capacitor is one of P capacitors, and wherein a capacitance of each of the P capacitors is included in the associated capacitance of at least one of the N drivers.

26. (original) The converter of claim 25, wherein P is less than N.

27. (original) The converter of claim 25, wherein P is greater than or equal to N.

28. (original) The converter of claim 23, wherein the integrated circuit further comprises a second multi-level controller in communication with the second control terminal, the second multi-level controller including M drivers, each of

the m=1 to m=M drivers to selectively apply a different voltage V_m to the second control terminal, where M is greater than two.

29. (original) The controller of claim 23, wherein the first switch comprises a first transistor, the first control terminal comprises a gate of the first transistor, and wherein a first driver is to selectively apply a voltage V_1 to the gate of the first transistor sufficient to turn on the transistor, to selectively apply a voltage V_3 to the gate of the first transistor sufficient to turn off the transistor, and to selectively apply a voltage V_2 between V_1 and V_3 to the gate of the first transistor.

30. (original) A direct current to direct current converter, comprising:

a first switching assembly, the first switching assembly including I switches, each of the I switches to output a voltage on an associated output terminal in response to a turn-on voltage at an associated control terminal, each of the associated output terminals in communication with a first switching assembly output terminal configured to output a voltage to a load, one or more of the I switches further including an associated multi-level controller in communication with an associated control terminal, an i-th one of the

associated multi-level controllers including N(i) drivers, each of the n(i)=1 to n(i)=N(i) drivers to selectively apply a different voltage $V_{n(i)}$ to the associated control terminal, where N(i) is greater than two for at least one of the I switches.

31. (original) The converter of claim 30, further comprising:

a second switching assembly, the second switching assembly including J switches, each of the J switches to output a voltage on an associated output terminal in response to a turn-on voltage at an associated control terminal, each of the associated output terminals in communication with a second switching assembly output terminal in communication with the first switching assembly output terminal, one or more of the J switches further including an associated multi-level controller in communication with an associated control terminal, a j-th one of the associated multi-level controllers including N(j) drivers, each of the n(j)=1 to n(j)=N(j) drivers to selectively apply a different voltage $V_{n(j)}$ to the associated control terminal, where N(j) is greater than two for at least one of the J switches.

32. (original) The converter of claim 30, wherein the I switches comprise I transistors, and wherein the associated control terminal comprises a gate of the associated transistor.

33. (original) The converter of claim 30, wherein each of the I switches includes an associated multi-level controller in communication with the associated control terminal.

34. (original) The converter of claim 30, wherein N(i) is the same for each of the associated multi-level controllers.

35. (original) The converter of claim 30, wherein N(i) is different for at least some of the associated multi-level controllers.

36. (original) A method of direct current to direct current power conversion, the method comprising:

alternately generating a first output voltage at an output of a first switching assembly including I switches and generating a second output voltage at an output of a second switching assembly including J switches, the output of the first switching assembly in communication with the output of the second switching assembly, wherein generating the first output

voltage comprises turning on the first switching assembly, and wherein turning on the first switching assembly comprises:

selectively applying n(i)=1 to n(i)=N(i) different voltages $V_{n(i)}$ to an associated control terminal of an i-th one of the I switches, wherein selectively applying the different voltages $V_{n(i)}$ comprises applying a voltage $V_{1(i)}$ at which the i-th switch is off, subsequently applying an intermediate voltage $V_{int(i)}$, and subsequently applying a voltage $V_{N(i)}$ at which the i-th switch is on, wherein $V_{int(i)}$ is between $V_{1(i)}$ and $V_{N(i)}$.

37. (original) The method of claim 36, wherein generating the second output voltage comprises turning on the second switching assembly, and wherein turning on the second switching assembly comprises:

selectively applying m(j)=1 to m(j)=M(j) different voltages $V_{m(j)}$ to an associated control terminal of a j-th one of the J switches, wherein selectively applying the different voltages $V_{m(j)}$ comprises applying a voltage $V_{1(j)}$ at which the j-th switch is off, subsequently applying an intermediate voltage $V_{int(j)}$, and subsequently applying a voltage $V_{M(j)}$ at which the j-th switch is on, wherein $V_{int(j)}$ is between $V_{1(j)}$ and $V_{M(j)}$.

38. (original) The method of claim 36, further comprising filtering the first output voltage and the second output voltage to produce a generally direct current voltage.

39. (original) The method of claim 38, further comprising applying the generally direct current voltage to a load.

40. (original) The method of claim 36, wherein turning on the first switching assembly comprises selectively applying a voltage $V_{2(i)}=V_2$ in turn to a plurality of the I switches and applying a voltage $V_{3(i)}=V_3$ to the plurality of the I switches.

41. (original) The method of claim 40, wherein selectively applying the voltage V_2 in turn to the plurality of the I switches and applying the voltage V_3 to the plurality of the I switches comprises applying the voltage V_3 to at least one of the plurality of I switches and applying the voltage V_2 to a different one of the plurality of I switches at the same time.

42. (original) The method of claim 40, wherein selectively applying the voltage V_2 in turn to the plurality of the I switches comprises applying the voltage V_2 to each of the i=1 to i=I switches sequentially, and wherein applying the voltage V_3 to the plurality of the I switches comprises applying the voltage V_3

to each of the I switches sequentially, and wherein applying the voltage V_3 to at least one of the plurality of I switches and applying the voltage V_2 to a different one of the plurality of I switches at the same time comprises applying the voltage V_3 to the i=1 switch prior to applying the voltage V_2 to the i=I switch.

43. (original) The method of claim 36, wherein generating the second output voltage comprises turning on the second switching assembly, and wherein turning on the second switching assembly comprises:

selectively applying m(j)=1 to m(j)=M(j) different voltages $V_{m(j)}$ to an associated control terminal of a j-th one of the J switches, wherein selectively applying the different voltages $V_{m(j)}$ comprises applying a voltage $V_{1(j)}$ at which the j-th switch is off, subsequently applying an intermediate voltage $V_{int(j)}$, and subsequently applying a voltage $V_{M(j)}$ at which the j-th switch is on, wherein $V_{int(j)}$ is between $V_{1(j)}$ and $V_{M(j)}$; and

wherein alternately generating the first output voltage at the output of the first switching assembly and generating the second output voltage at the output of the second switching assembly comprises turning on the first switching assembly while selectively applying a voltage $V_{off(j)}$ to each of the j=1 to j=J

switches, where $V_{off(j)}$ is a voltage at which the respective j-th switch is off.

44. (original) The method of claim 36, wherein generating the second output voltage comprises turning on the second switching assembly, and wherein turning on the second switching assembly comprises:

selectively applying m(j)=1 to m(j)=M(j) different voltages $V_{m(j)}$ to an associated control terminal of a j-th one of the J switches, wherein selectively applying the different voltages $V_{m(j)}$ comprises applying a voltage $V_{1(j)}$ at which the j-th switch is off, subsequently applying an intermediate voltage $V_{int(j)}$, and subsequently applying a voltage $V_{M(j)}$ at which the j-th switch is on, wherein $V_{int(j)}$ is between $V_{1(j)}$ and $V_{M(j)}$; and

wherein alternately generating the first output voltage at the output of the first switching assembly and generating the second output voltage at the output of the second switching assembly comprises turning on the first switching assembly while selectively applying a voltage different than $V_{1(j)}$ to at least one of the j=1 to j=J switches.

45. (original) The method of claim 44, wherein the voltage different than $V_1(j)$ is $V_2(j)$.

46. (original) The method of claim 36, wherein $V_{2(j)}$ is a voltage at which the respective at least one of the j=1 to j=J switches is barely on.

47. (original) A direct current to direct current converter, comprising:

means for generating a first output voltage at a node of the direct current to direct current converter;

means for generating a second output voltage alternately with the first output voltage at the node;

wherein the means for generating the first output voltage comprises:

means for selectively applying n=1 to n=N(i) different voltages to a control terminal of an i-th one of I switches, wherein the different voltages include a voltage V_{1i} at which the associated i-th switch is off, a voltage $V_{N(i)i}$ at which the associated i-th switch is on, and a voltage $V_{int(i)}$ between V_{1i} and $V_{N(i)i}$.

48. (original) The converter of claim 47, wherein the means for generating the first output voltage comprises:

means for selectively applying m=1 to m=M(j) different voltages to a control terminal of a j-th one of J switches, wherein the different voltages include a voltage V_{1j} at which the

associated j-th switch is off, a voltage $V_{M(j)j}$ at which the associated j-th switch is on, and $V_{int(j)}$ between V_{1j} and $V_{M(j)j}$.

49. (original) A direct current to direct current converter, comprising:

a first switching means, the first switching means for outputting a first voltage on a first output terminal means in response to a turn-on voltage at a first control terminal means, wherein the first control terminal means selectively communicates with one of N > 2 different voltages; and

a second switching means, the second switch for outputting a second voltage on a second output terminal means in communication with the first output terminal means in response to a turn-on voltage at a second control terminal means, wherein the second control terminal means selectively communicates with one of M > 1 different voltages.

50. (original) The converter of claim 49, wherein M is greater than two.

51. (original) The converter of claim 49, wherein the first output terminal means and the second output terminal means are in communication with a load.

52. (original) The converter of claim 51, wherein the first output terminal means and the second output terminal means are in communication with the load via an inductor and a capacitor.

53. (original) The converter of claim 49, wherein the first switching means comprises a first transistor, the first output terminal means comprises a drain of the first transistor, and the first control terminal means comprises a gate of the first transistor.

54. (original) The converter of claim 49, further including a means for supplying each of the N different voltages.

55. (original) The converter of claim 49, wherein the first switching means comprises a transistor having a source and a drain, and further comprising a voltage detection means for detecting a potential difference between the source and the drain.

56. (original) The converter of claim 55, further including a switch assembly controlling means in communication with the voltage detection means and further in communication

with the first control terminal means, the switch assembly controlling means for comparing the potential difference between the source and the drain with a threshold potential difference, the switch assembly controlling means further for causing the first control terminal means to selectively communicate with a different one of the N > 2 different voltages if the potential difference between the source and the drain is less than the threshold potential difference.

57. (original) The converter of claim 49, further including a first multi-level controlling means for controlling the first switching means, the first multi-level controlling means in communication with the first control terminal, the first multi-level controlling means including N driving means, each of the n=1 to n=N driving means for selectively applying a different voltage V_n of the N different voltages to the first control terminal means.

58. (original) The converter of claim 57, further including a second multi-level controlling means for controlling the second switching means, the second multi-level controlling means in communication with the second control terminal means, the second multi-level controlling means including M driving means, each of the m=1 to m=M driving means for selectively

applying a different voltage V_m of the M different voltages to the second control terminal means.

59. (original) The converter of claim 58, wherein the first multi-level controlling means and the second multi-level controlling means are for turning on the first switching means and the second switching means alternately.

60. (original) The converter of claim 57, wherein the first multi-level controlling means comprises a switching means for selectively communicating the N > 2 different applied voltages with the first control terminal means.

61. (original) The converter of claim 57, wherein at least one of the N driving means comprises an associated capacitance.

62. (original) The converter of claim 61, wherein at least a portion of the first multi-level controlling means is included in an integrated circuit, and wherein an associated capacitance of at least one of the N driving means includes a capacitance of a capacitor not included in the integrated circuit.

63. (original) The converter of claim 62, wherein the first switching means comprises a transistor with a gate and a

source having an associated capacitance C_{gs}, and wherein the capacitance of the capacitor not included in the integrated circuit is larger than C_{gs}.

64. (original) The converter of claim 57, wherein the first switching means comprises a PMOS transistor, wherein the first control terminal means is a gate of the PMOS transistor, and wherein the N driving means comprise three driving means for selectively applying a voltage V_1 at which the PMOS transistor is off, a voltage V_3 at which the PMOS transistor is on, and an intermediate voltage V_2 between V_1 and V_3.

65. (original) The converter of claim 64, wherein V_1 is about equal to negative five volts or less, and wherein V_3 is ground.

66. (original) The converter of claim 64, wherein the N driving means further comprise a fourth driving means for selectively applying another intermediate voltage V_4, and wherein V_4 is between V_1 and V_3.

67. (original) The converter of claim 57, wherein the first switching means comprises an NMOS transistor, wherein the first control terminal means is a gate of the NMOS transistor,

and wherein the N driving means comprise three driving means for selectively applying a voltage V_1 at which the NMOS transistor is on, a voltage V_3 at which the NMOS transistor is off, and an intermediate voltage V_2 between V_1 and V_3.

68. (original) The converter of claim 67, wherein V_1 is equal to about five volts or greater, and wherein V_3 ground.

69. (original) The converter of claim 67, wherein the N driving means further comprise a fourth driving means for selectively applying another intermediate voltage V_4, and wherein V_4 is between V_1 and V_3.

70. (original) The converter of claim 57, wherein the N driving means are for selectively applying the different voltage V_n for a time sufficient for the voltage at the first control terminal means to substantially equilibrate with V_n.

71. (original) A direct current to direct current converter, comprising:

an integrated circuit, the integrated circuit including:

a first switching means, the first switching means for outputting a first voltage on a first output

terminal means in response to a turn-on voltage at a first control terminal means;

a second switching means, the second switching means for outputting a second voltage on a second output terminal means in communication with the first output terminal means in response to a turn-on voltage at a second control terminal means; and

a first multi-level controlling means for controlling the first switching means, the first multi-level controlling means in communication with the first control terminal means, the first multi-level controlling means including N driving means, each of the n=1 to n=N driving means for selectively applying a different voltage V_n to the first control terminal means, where N is greater than two, and wherein at least one of the N driving means comprises an associated capacitance means; and

a second capacitance means separate from the integrated circuit, a capacitance of the second capacitance means included in the associated capacitance means of one of the N driving means.

72. (original) The converter of claim 71, wherein the associated capacitance means of the one of the N driving means

further includes an on-chip capacitance of one or more elements of the integrated circuit.

73. (original) The converter of claim 71, wherein the second capacitance means includes one of P capacitors, and wherein a capacitance of each of the P capacitors is included in the associated capacitance means of at least one of the N driving means.

74. (original) The converter of claim 73, wherein P is less than N.

75. (original) The converter of claim 73, wherein P is greater than or equal to N.

76. (original) The converter of claim 71, wherein the integrated circuit further comprises a second multi-level controlling means for controlling the second switching means, the second multi-level controlling means in communication with the second control terminal means, the second multi-level controlling means including M driving means, each of the m=1 to m=M driving means for selectively applying a different voltage V_m to the second control terminal means, where M is greater than two.

77. (original) The controller of claim 71, wherein the first switching means comprises a first transistor, the first control terminal means comprises a gate of the first transistor, and wherein a first driving means is for selectively applying a voltage V_1 to the gate of the first transistor sufficient to turn on the transistor, for selectively applying a voltage V_3 to the gate of the first transistor sufficient to turn off the transistor, and for selectively applying a voltage V_2 between V_1 and V_3 to the gate of the first transistor.

78. (original) A direct current to direct current converter, comprising:

a first switching assembly means, the first switching assembly means including I switching means, each of the I switching means for outputting a voltage on an associated output terminal means in response to a turn-on voltage at an associated control terminal means, each of the associated output terminal means in communication with a first switching assembly means output terminal means configured to output a voltage to a load, one or more of the I switching means further including an associated multi-level controlling means for controlling the switching means, the associated multi-level controlling means in communication with an associated control terminal means, an i-th

one of the associated multi-level controlling means including N(i) driving means, each of the n(i)=1 to n(i)=N(i) driving means for selectively applying a different voltage $V_{n(i)}$ to the associated control terminal means, where N(i) is greater than two for at least one of the I switching means.

79. (original) The converter of claim 78, further comprising:

a second switching assembly means, the second switching assembly means including J switching means, each of the J switching means to output a voltage on an associated output terminal means in response to a turn-on voltage at an associated control terminal means, each of the associated output terminal means in communication with a second switching assembly means output terminal means in communication with the first switching assembly means output terminal means, one or more of the J switching means further including an associated multi-level controlling means for controlling the switching means, the associated multi-level controlling means in communication with an associated control terminal means, a j-th one of the associated multi-level controlling means including N(j) driving means, each of the n(j)=1 to n(j)=N(j) driving means for selectively applying a different voltage $V_{n(j)}$ to the associated

control terminal means, where N(j) is greater than two for at least one of the J switches.

80. (original) The converter of claim 78, wherein the I switching means comprise I transistors, and wherein the associated control terminal means comprises a gate of the associated transistor.

81. (original) The converter of claim 78, wherein each of the I switching means includes an associated multi-level controlling means in communication with the associated control terminal means.

82. (original) The converter of claim 78, wherein N(i) is the same for each of the associated multi-level controlling means.

83. (original) The converter of claim 78, wherein N(i) is different for at least some of the associated multi-level controlling means.

84. (new) The converter of claim 1, wherein the first control terminal selectively communicates with one of N > 2 different voltages sequentially.

85. (new) The converter of claim 23, wherein the first multi-level controller includes the N drivers configured such that each of the n=1 to n=N drivers selectively and sequentially applies a different voltage V_n to the first control terminal.

86. (new) The converter of claim 30, wherein the i-th one of the associated multi-level controllers includes the N(i) drivers configured such that each of the n(i)=1 to n(i)=N(i) drivers selectively and sequentially applies a different voltage $V_{n(i)}$ to the associated control terminal.

87. (new) The converter of claim 47, wherein the means for selectively applying comprises means for selectively and sequentially applying the n=1 to n=N(i) different voltages to the control terminal of the i-th one of the I switches.

88. (new) The converter of claim 49, wherein the first control terminal means selectively and sequentially communicates with one of N > 2 different voltages.

89. (new) The converter of claim 71, wherein the n=1 to n=N driving means comprises n=1 to n=N driving means for

selectively and sequentially applying a different voltage V_n to the first control terminal means.

90. (new) The converter of claim 78, wherein the n(i)=1 to n(i)=N(i) driving means comprises n(i)=1 to n(i)=N(i) driving means for selectively and sequentially applying a different voltage $V_{n(i)}$ to the associated control terminal means.